A Three-Level T-Type Indirect Matrix Converter Based on the Third-Harmonic Injection Technique

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***Abstract*— An indirect matrix converter (IMC) is a direct ac-ac power converter. As an improvement of the output waveform quality, several types of three-level IMC are proposed and investigated. However, two major problems of these converters still exist. First, in some specific situations, such as wind energy conversion systems and flexible ac transmission systems, these converters' capabilities of generating input reactive power must be improved greatly. Second, neutral-point voltage balancing is a key challenge to the normal operation of multilevel IMCs, but the control of balancing the neutral-point voltage for multilevel IMCs has not been investigated so far. To address these issues, a three-level T-type indirect MC (3LT^{2}IMC) topology as well as a carrier-based modulation method is proposed. In addition to inheriting the advantages of the third-harmonic injection two-stage MC such as extended input reactive power control range and no need for synchronization in modulation, 3LT^{2}IMC could provide an improved output power quality. Besides, a closed-loop control algorithm for balancing the neutral-point voltage is developed. The presented modulation strategy and control algorithm are generalized and can be extended to other three-level IMCs. Finally, the proposed topology and method are verified by simulation and experimental results.**

***Index Terms*— AC-AC power conversion, neutral-point voltage balancing, third-harmonic injection, three-level t-type indirect matrix converter (3LT^{2}IMC).**

I. Introduction

A MATRIX converter (MC) is an "all-semiconductor" direct ac-ac power converter, which is featured by the advantages such as bidirectional power flow, sinusoidal input and output currents, controllable input power factor as well as high power density. Due to the merits described above, MCs have attracted an increasing attention in recent years [1]–[7].

As an improvement of the output waveform quality, the multilevel converter concept has been applied to MCs [6], [8]–[18]. With the ability to synthesize multilevel output voltages, the multilevel MCs could achieve better output power quality, reduced voltage stress on the power switches and lower *du*/*dt* stresses when compared with the conventional two-level MCs. Generally, the multilevel MCs could be classified as three categories: the multimodular MCs [8]–[10], the capacitor clamped MCs [11]–[13] and the neutral-point clamped (NPC) MCs (also known as the multilevel IMCs) [6], [14]–[18]. The multi-modular MC is formed by cascaded three-phase to single-phase MC modules, and it has the advantages of good output power quality and flexible expansibility, but a bulky multiwinding transformer is necessary. The capacitor clamped MC utilizes flying capacitors to provide the middle voltage levels so as to produce multi-level output voltages. A drawback of the capacitor clamped MC is the need of excessive numbers of capacitors and complicated control methods to balance the flying capacitor voltages.

As for the NPC MC, it is derived from the indirect MC (IMC). Thus, except the ability to generate multilevel output voltages and the possibility of achieving higher conversion efficiency, the NPC MCs also inherit the advantages of IMCs such as simple commutation mechanism and clamp circuit. These advantages make NPC MCs an attractive choice in some applications. In [6], a three-level-output-stage MC (3MC) topology has been proposed, and the operating principles and space vector modulation (SVM) scheme of 3MC have been investigated in [14]. However, the developed nearest three virtual SVM aiming at maintaining zero averaged neutral-point current has the drawbacks of relatively high computational burden and nonzero-current commutation of the rectifier. In [15], a carrier-based modulation scheme for 3MC has been presented, and the performances of 3MC have been verified experimentally. Another three-level IMC topology, referred to as the indirect three-level sparse MC (I3SMC), has been proposed and studied in [16] and [17]. Compared with 3MC, the I3SMC topology has the advantage of a reduced number of switches, but at the cost of a slight degradation of the output performance due to the absence of the medium voltage vectors when synthesizing the output voltages. In [18], a three-level diode-clamped MC has been suggested, which consists of a cascaded-rectifier and a three-level diode-clamped inverter.

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Although the three-level diode-clamped MC can be easily extended to a generalized multilevel IMC topology, the bulky multiwinding isolated transformer reduces the power density of the converter inevitably.

Besides advantages, multilevel IMCs derived from IMCs also inherit the drawbacks of the conventional IMCs: One is the limited ability to generate input reactive power. The other is the need for synchronization in modulation between the rectification stage and the inversion stage. The first one is more obvious when multilevel IMCs are applied in a wind energy conversion system (WECS) or a flexible ac transmission system (FACTS) [19], [20]. The input reactive power of multilevel IMCs can be regulated to some extent by changing the input displacement angle, but at the cost of a reduced maximum voltage transfer ratio, which is similar to that of IMCs [21], [22]. For the second, the input and output power quality of multilevel IMCs may degrade [23], since the process of synthesizing the output voltage vector occurs in two time-varying subperiods of the rectification stage, and modulation of the inversion stage is difficult to realize when the desired input current vector is located in the sector boundaries.

On the other hand, similar to the conventional NPC converters, neutral-point voltage balancing is a key challenge to the normal operation of multilevel IMCs. The neutral-point voltage imbalance problem in multilevel IMC may become even worse than that of conventional NPC converters with bulky buffer capacitors, since the capacitance of the input capacitors providing the major energy storage is relatively small. For the 3MC and I3SMC topologies studied in [19]–[22], although natural-balancing of the neutral-point voltage under ideal conditions can be achieved through proper modulation strategies, the nonlinearities in the practical converter such as the nonidealities of the switches, the dead times effect and the transients, may cause the neutral-point potential drift and distort the output waveforms. For the three-level diode-clamped MC presented in [23], the leakage inductance of the isolated transformer may disrupt the self-balance of the neutral-point voltage, since zero averaged neutral-point current cannot be guaranteed by the modulation scheme. As far as we know, the control algorithm for balancing the neutral-point voltage of multilevel IMCs has not been discussed.

In this paper, a three-level T-type indirect MC (3LT^{2}IMC) topology is presented and investigated systematically, which is derived from the third-harmonic injection two-stage MC (3TSMC) [24]–[26] shown in Fig. 1. In addition to possessing the inherent advantages of 3TSMC such as bidirectional power flow capability, sinusoidal inputs and outputs, extended input reactive power control range without lowing the maximum voltage transfer ratio and no need for synchronization between the rectification stage and inversion stage, 3LT^{2}IMC could provide an improved output power quality in terms of output harmonic contents. The topology and operating principles of 3LT^{2}IMC are analyzed in detail. Based on the analysis of the operating principles, a simple carrier-based modulation method is introduced. Moreover, a closed-loop control algorithm for balancing the neutral-point voltage is developed, which overcomes the neutral-point potential drift issue caused by the nonidealities of the practical converter. Finally, the proposed topology and method are verified by simulation and experimental studies, and a comprehensive performance comparison with 3TSMC is carried out. This paper is organized as follows: Section II introduces the topology and operating principles of 3LT^{2}IMC; Section III presents the carrier-based modulation scheme in detail; Section IV analyzes the factors that influence the balance of the neutral-point voltage in practice, followed by the presentation of the control algorithm for balancing the neutral-point voltage; Section V shows the simulation and experimental results to verify the presented methods and gives a comprehensive performance comparison with 3TSMC; Section VI draws the final conclusion of this paper.

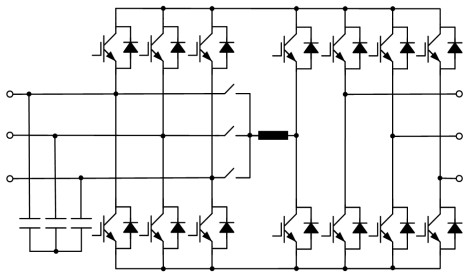

Fig. 1. 3TSMC topology.

II. Topology and Operating Principles of 3LT^{2}IMC

A. Topology

The topology of 3LT^{2}IMC is shown in Fig. 2, the main circuit consists of a bidirectional current-source-type rectifier (CSR), a three-level voltage-source-type inverter (VSI), an active third-harmonic current injection circuit, and an input *LC* filter. Compared with 3TSMC shown in Fig. 1, the CSR of 3LT^{2}IMC is cascaded to a three-level T-type VSI instead of the conventional two-level VSI. The active third-harmonic current injection circuit is composed of three bidirectional switches, a third-harmonic injection inductor and a bridge leg. The input filter consisting of inductor L_F and film capacitor C_F mainly has three functions. First, it is used for filtering the pulse currents generated by the converter so as to produce three-phase sinusoidal input currents. Second, the star point of the capacitors in the filter provides the neutral point of the rear-end three-level T-type inverter. Third, as with the clamp circuit of the conventional IMCs, the capacitors of the filter are used for absorbing the energy stored in the leakage inductance of the load and the third-harmonic injection inductor when the converter shutdown. It should be noted that, although the three-level T-type inverter is used in the proposed topology shown in Fig. 2, other three-level NPC inverters such as the three-level diode-clamped inverter, can also be adopted here for implementing 3LT^{2}IMC. This can be realized by reallocating the gating signals of the inversion stage, therefore it is not elaborated here for clarity.

B. Operating Principles

Assume the three-phase input voltages are symmetrical and sinusoidal, the operating principles of 3LT^{2}IMC are

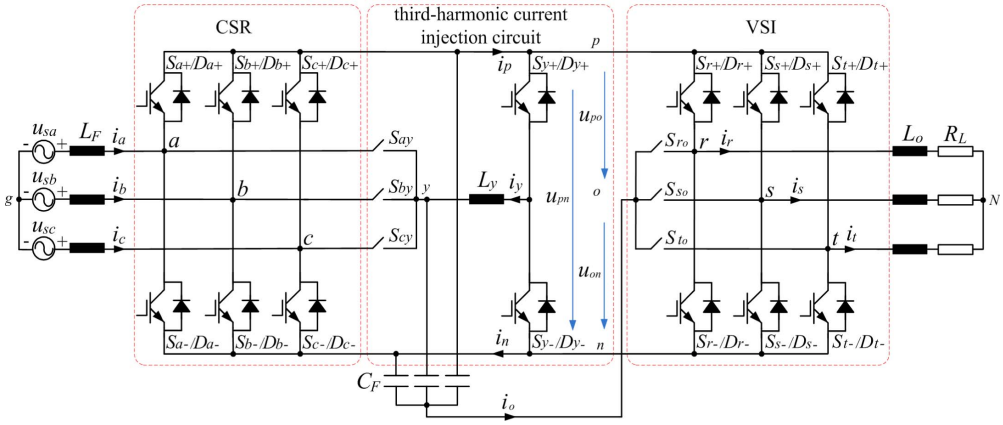

Fig. 2. Schematic of 3LT^{2}IMC topology.

TABLE I

SWITCHING STATES OF THE RECTIFIER AND THE THIRD-HARMONIC CURRENT INJECTION CIRCUIT

θ_{sa}	sector	S_{ay}	S_{by}	S_{cy}	S_{a+}	S_{a-}	S_{b+}	S_{b-}	S_{c+}	S_{c-}
0-π/3	1	0	1	0	1	0	0	0	0	1
π/3-2π/3	2	1	0	0	0	0	1	0	0	1
2π/3-π	3	0	0	1	0	1	1	0	0	0
π-4π/3	4	0	1	0	0	1	0	0	1	0
4π/3-5π/3	5	1	0	0	0	0	0	1	1	0
5π/3-2π	6	0	0	1	1	0	0	1	0	0

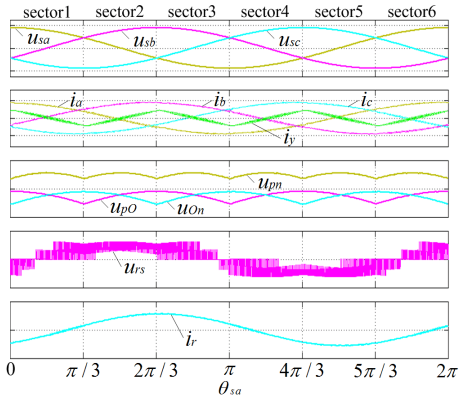

Fig. 3. Key waveforms of 3LT^{2}IMC.

described as follows: for the CSR, only the switch in the upper bridge connected to the input phase with the maximum instantaneous voltage, and the switch in the lower bridge connected to the input phase with the minimum instantaneous voltage, are turned on so as to impose two of the three phase-to-neutral voltages (labeled as u_{aO}, u_{bO}, and u_{cO}) across the intermediate dc link. For the third-harmonic current injection circuit, switches S_{y+} and S_{y-} are controlled to generate the desired quasi-third-harmonic current i_y flowing through the inductor L_y; and the bidirectional switch that connected to the input phase with the minimum absolute voltage, is turned on to inject the third-harmonic current i_y into the corresponding input phase. Table I shows the switching states of the CSR and the bidirectional switches of the third-harmonic current injection circuit, where θ_{sa} is the phase of the input phase voltage u_{sa}. For example, when the input voltages satisfy $u_{sa} > u_{sb} > u_{sc}$ (denoted as sector 1), switches S_{a+} and S_{c-} of the rectifier and the bidirectional switch S_{by} of the third-harmonic current injection circuit are turned on, node a connects to the positive terminal p and node c connects to the negative terminal n of the dc link. Thus the upper dc source voltage u_{pO} and the lower dc source voltage u_{On} are represented by the phase-to-neutral voltage u_{aO} and $-u_{cO}$, respectively, and so forth. Consequently, as with the output voltage of a diode rectifier, the dc link voltage u_{pn} of 3LT^{2}IMC exhibits a piecewise six-pulse shape waveform.

According to the requirements of the load, the three-level T-type inverter provides three-phase three-level output voltages with variable frequency and amplitude. In this manner, sinusoidal three-phase input–output currents and controllable input power factor are attainable. Fig. 3 shows the key waveforms of 3LT^{2}IMC, where u_{rs} is the output line-line voltage and i_r is the output current. The validity of sinusoidal currents and controllable power factor at the input side has been presented in detail in [25] and therefore is not elaborated here.

As can be seen from Fig. 3, different from the conventional T-type VSI, the split dc source of the T-type VSI in 3LT^{2}IMC is no longer to have balanced upper and lower dc voltages. Instead, the upper and lower dc voltages in each sector are now represented by two different input phase-to-neutral voltages. Consequently, as will be explained in the next section, the modulation strategies of the traditional T-type VSI cannot be directly used here, and proper modifications should be made for achieving symmetrical and sinusoidal input and output waveforms.

III. CARRIER-BASED MODULATION METHOD

Similar to 3TSMC, the modulation strategies of the developed 3LT^{2}IMC can also be divided into two independent parts. Since the switching states of the rectifier and the bidirectional switches of the third-harmonic current injection circuit are

determined only by the input voltages, they commutate at line frequency, and the modulation strategies of the rectifier and the third-harmonic current injection circuit are relatively simple, as shown in Table I. For the rear-end T-type VSI, a carrier-based double-signal pulsewidth modulation method (DSPWM) [27], [28] is developed for reducing the computational burden, and the concrete analysis is given as follows.

Assume the symmetrical three-phase output reference voltages, also known as the modulation signals, are given by

$$\begin{cases} u_r^* = U_{\text{om}}\cos(\omega_o t + \phi) \\ u_s^* = U_{\text{om}}\cos(\omega_o t - 2\pi/3 + \phi) \\ u_t^* = U_{\text{om}}\cos(\omega_o t + 2\pi/3 + \phi) \end{cases} \tag{1}$$

where u_r^*, u_s^*, and u_t^* are the three modulation signals, U_{om}, ω_o, and ϕ are the magnitude, angular frequency and initial phase of the expected output voltages, respectively.

First, sort the original modulation signals according to the instantaneous values of the expected output voltages as follows:

$$\begin{cases} u_{\text{max}}^* = \max(u_r^*, u_s^*, u_t^*) \\ u_{\text{mid}}^* = \text{mid}(u_r^*, u_s^*, u_t^*) \\ u_{\text{min}}^* = \min(u_r^*, u_s^*, u_t^*) \end{cases} \tag{2}$$

where u_{max}^*,u_{mid}^*,and u_{min}^* represent the maximum value, medium value and minimum value among the modulation signals; max(), mid(), and min() are the operators of the maximum value, medium value and minimum value, respectively.

To achieve the maximum range of linear voltage transfer ratio for 3LT^{2}IMC, each original modulation signal is modified by adding a common zero-sequence voltage

$$\begin{cases} u_{\text{max}}^{*'} = u_{\text{max}}^* + u_0 \\ u_{\text{mid}}^{*'} = u_{\text{mid}}^* + u_0 \\ u_{\text{min}}^{*'} = u_{\text{min}}^* + u_0 \end{cases} \tag{3}$$

where u_0 is the zero-sequence voltage, and $u_{\text{max}}^{*'}$, $u_{\text{mid}}^{*'}$, and $u_{\text{min}}^{*'}$ are the modified modulation signals.

According to DSPWM, the modified modulation signals are then decomposed into two modulation signals for achieving zero averaged neutral-point current. Denote $u_{\text{max}p}^*$, $u_{\text{mid}p}^*$, and $u_{\text{min}p}^*$ as the positive modulation signals corresponding to the maximum, medium and minimum original modulation signals, respectively; $u_{\text{max}n}^*$, $u_{\text{mid}n}^*$, and $u_{\text{min}n}^*$ are the negative modulation signals corresponding to the maximum, medium and minimum original modulation signals, respectively, then the modified modulation signals are

$$\begin{cases} u_{\text{max}}^{*'} = u_{\text{max}p}^* + u_{\text{max}n}^* \\ u_{\text{mid}}^{*'} = u_{\text{mid}p}^* + u_{\text{mid}n}^* \\ u_{\text{min}n}^{*'} = u_{\text{min}p}^* + u_{\text{min}n}^* \end{cases} \tag{4}$$

$$\begin{cases} u_{\text{max}p}^* = u_{\text{max}}^* + u_{0,} \\ u_{\text{max}n}^* = 0 \\ u_{\text{mid}p}^* = 0.5u_{\text{mid}}^* + u_{01}, \\ u_{\text{mid}n}^* = 0.5u_{\text{mid}}^* + u_{02} \\ u_{\text{min}p}^* = 0, \\ u_{\text{min}n}^* = u_{\text{min}}^* + u_0 \end{cases} \tag{5}$$

where u_{01} and u_{02} are the zero-sequence voltages of the positive and negative modulation signals corresponding to the medium original modulation signal, respectively.

For the convenience of digital implementation, the positive and negative modulation signals are normalized according to the upper and lower dc voltages, respectively. The normalized modulation signals and the duty ratios are determined by

$$\begin{cases} \bar{u}_{\text{ip}}^* = u_{\text{ip}}^*/u_{pO} \\ \bar{u}_{\text{in}}^* = u_{\text{in}}^*/u_{\text{On}}, \end{cases} \quad i \in \{\text{max, mid, min}\} \tag{6}$$

$$\begin{cases} d_{\text{ip}} = \bar{u}_{\text{ip}}^* \\ d_{\text{in}} = -\bar{u}_{\text{in}}^*, \end{cases} \quad i \in \{\text{max, mid, min}\} \tag{7}$$

where $\bar{u}_{\text{ip}}^*$ are the normalized positive modulation signals, $\bar{u}_{\text{in}}^*$ are the normalized negative modulation signals, d_{ip} represent the duty ratios connected to the positive terminal of the dc link, and d_{in} denote the duty ratios connected to the negative terminal of the dc link.

To eliminate the low-frequency oscillations of the neutral-point voltage, the averaged neutral-point current in each switching period (denoted as $\bar{i}_O$) must be kept at zero. Thus, the zero-sequence voltages to ensure zero averaged neutral-point current could be solved from the following equations:

$$\begin{cases} \bar{i}_O = (1 - d_{\text{max}p})i_{\text{max}} + (1 - d_{\text{mid}p} - d_{\text{mid}n})i_{\text{mid}} \\ \qquad + (1 - d_{\text{min}n})i_{\text{min}} = 0 \\ i_{\text{max}} + i_{\text{mid}} + i_{\text{min}} = 0 \\ u_{\text{max}}^* + u_{\text{mid}}^* + u_{\text{min}}^* = 0 \\ u_0 = u_{01} + u_{02} \end{cases} \tag{8}$$

with the constraints

$$\begin{cases} 0 \le u_{\text{max}p}^* \le u_{pO} \\ 0 \le u_{\text{mid}p}^* \le u_{pO} \\ -u_{\text{On}} \le u_{\text{mid}n}^* \le 0 \\ -u_{\text{On}} \le u_{\text{min}n}^* \le 0 \end{cases} \tag{9}$$

where i_{max}, i_{mid}, and i_{min} represent the output currents corresponding to the phase having the maximum, medium and minimum original modulation signals, respectively.

One set of feasible choice of the zero-sequence voltages is given by

$$\begin{cases} u_{01} = \dfrac{-0.5u_{\text{mid}}^*(u_{\text{On}} - u_{pO}) - u_{pO}u_{\text{min}}^*}{u_{pn}} \\ u_{02} = \dfrac{0.5u_{\text{mid}}^*(u_{\text{On}} - u_{pO}) - u_{\text{On}}u_{\text{max}}^*}{u_{pn}} \\ u_0 = \dfrac{-u_{pO}u_{\text{min}}^* - u_{\text{On}}u_{\text{max}}^*}{u_{pn}}. \end{cases} \tag{10}$$

Substitute (10) into (5), the unified expression of the normalized modulation signals is given by

$$\begin{cases} \bar{u}_{\text{ip}}^* = (u_i^* - u_{\text{min}}^*)/u_{pn} \\ \bar{u}_{\text{in}}^* = (u_i^* - u_{\text{max}}^*)/u_{pn}, \end{cases} \quad i \in \{\text{max, mid, min}\}. \tag{11}$$

Under the condition of $u_r^* = u_{\text{max}}^*, u_s^* = u_{\text{mid}}^*, u_t^* = u_{\text{min}}^*$, Fig. 4 shows the schematic and switching pattern of the modulation scheme for the inverter of 3LT^{2}IMC, where T_s is the switching period, f_s is the switching frequency,

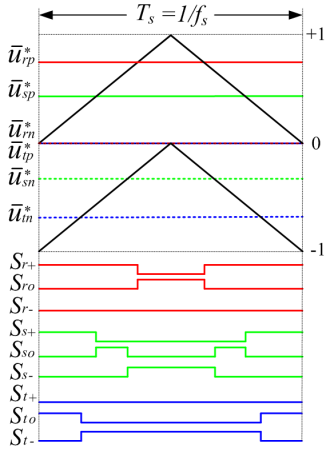

Fig. 4. Schematic and switching pattern of the modulation scheme for the inverter of 3LT^{2}IMC.

$\bar{u}^*_{rp}$, $\bar{u}^*_{sp}$, and $\bar{u}^*_{tp}$ are the normalized positive modulation signals corresponding to the output phase r, s, and t, respectively, and $\bar{u}^*_{rn}$, $\bar{u}^*_{sn}$, and $\bar{u}^*_{tn}$ are the normalized negative modulation signals corresponding to the output phase r, s and t, respectively.

The voltage transfer characteristic is always the main concerns for IMCs. As a member of the IMCs family, the voltage transfer characteristic of 3LT^{2}IMC is deduced as follows.

Assume that the input voltages are given by

$$\begin{cases} u_{sa} = U_{\text{im}} \cos(\theta_{sa}) \\ u_{sb} = U_{\text{im}} \cos(\theta_{sa} - 2\pi/3) \\ u_{sc} = U_{\text{im}} \cos(\theta_{sa} + 2\pi/3) \end{cases} \tag{12}$$

where U_{im} is the magnitude of the input voltages. Ignoring the effects of the input filter, the dc link voltage u_{pn} can be written as

$$u_{pn} = \sqrt{3} U_{\text{im}} \cos\left[\text{rem}\left(\theta_{sa}, \frac{\pi}{3}\right) - \frac{\pi}{6}\right] \tag{13}$$

where rem() is the operator of the remainder value.

In linear modulation regions, the following conditions must be satisfied:

$$\begin{cases} 0 \le \bar{u}^*_{\text{ip}} \le 1 \\ -1 \le \bar{u}^*_{\text{in}} \le 0, \end{cases} \quad i \in \{\max, \text{mid}, \min\}. \tag{14}$$

Combine (1), (2), (4), (11), (13), and (14), the linear voltage transfer ratio of 3LT^{2}IMC could be derived as

$$q = \frac{U_{\text{om}}}{U_{\text{im}}} = \frac{\sqrt{3}}{2} m_i \le \frac{\sqrt{3}}{2} \tag{15}$$

where q is the linear voltage transfer ratio and m_i is the modulation index with the value range from 0 to 1. It can be found from (15) that the maximum linear voltage transfer ratio of 3LT^{2}IMC under all operation conditions is limited to 0.866, which is the same as that of 3TSMC.

IV. Control Algorithm for Balancing Neutral-Point Voltage

From the analysis in Section III it can be found that the developed modulation scheme for the T-type inverter possesses the feature of natural-balancing, since the average value of the neutral-point current in a switching period is zero under ideal conditions, as shown in (8). However, the nonlinearities of the practical converter such as the nonidealities of the devices, dead times effect, transients, etc., may cause the neutral-point potential drift and distort the output waveforms. Compared with the conventional NPC VSI with bulky buffer capacitors, the capacitance of the filtering capacitor of 3LT^{2}IMC is relatively small (usually in the range of several microfarads to tens of microfarads), and thus 3LT^{2}IMC is more susceptible to the disturbance of the neutral-point current. Consequently, as with the three-level VSIs with small dc link capacitors [28], a closed-loop control algorithm for balancing the neutral-point voltage is essential for the normal operation of 3LT^{2}IMC.

A. Dynamic Analysis of the Neutral-Point Voltage

Before designing a closed-loop controller for balancing the neutral-point voltage, the dynamic model of the neutral-point voltage should be obtained first. Using the circuit shown in Fig. 2, the mathematical model of the input filter is given by

$$\begin{cases} u_{sa} = L_F \dfrac{di_a}{dt} + u_{aO} + u_{Og} \\ u_{sb} = L_F \dfrac{di_b}{dt} + u_{bO} + u_{Og} \\ u_{sc} = L_F \dfrac{di_c}{dt} + u_{cO} + u_{Og} \\ i_O = C_F \dfrac{du_{aO}}{dt} + C_F \dfrac{du_{bO}}{dt} + C_F \dfrac{du_{cO}}{dt} \end{cases} \tag{16}$$

where u_{aO}, u_{bO} and u_{cO} are the voltages imposed across the filtering capacitors, and u_{Og} is the neutral-point voltage. For the symmetrical and sinusoidal three-phase system, the average state space model can be derived as

$$\frac{d\bar{u}_{Og}}{dt} = -\frac{\bar{i}_O}{3C_F} \tag{17}$$

where $\bar{u}_{Og}$ is the average value of the neutral-point voltage in a switching period.

It can be found from (17) that the neutral-point voltage variation is a function of the averaged neutral-point current. Thus the neutral-point voltage can be controlled by changing the averaged neutral-point current. It shows in the first formula of (8) that the averaged neutral-point current can be regulated by changing the modulation signals which in turn controls the neutral-point voltage. However, there are two criteria when modifying the modulation signals: 1) do not increase the switching frequency of the converter and 2) keep the expected output line-line voltages unchanged, which can be achieved by modifying the zero-sequence voltages of the modulation signals according to the discussion in Section III.

By introducing a new zero-sequence voltage u_{off}, the positive and negative modulation signals in (5) are

modified as

$$\begin{cases} u^{*'}_{\max p} = u^{*}_{\max p} + u_{\text{off}} \\ u^{*'}_{\max n} = 0 \\ u^{*'}_{\text{mid}p} = u^{*}_{\text{mid}p} + 0.5u_{\text{off}} \\ u^{*'}_{\text{mid}n} = u^{*}_{\text{mid}n} + 0.5u_{\text{off}} \\ u^{*'}_{\min p} = 0 \\ u^{*'}_{\min n} = u^{*}_{\min n} + u_{\text{off}} \end{cases} \tag{18}$$

where the symbol "′" represents the modified value. It can be verified easily from (18) that the expected output line-line voltages remain unchanged after modifying the modulation signals. Besides, (14) must be guaranteed to avoid distortions in the output voltages, which leads to the constraint condition of the new zero-sequence voltage u_{off} as follows:

$$\begin{cases} u_{\text{off}_{\min}} \le u_{\text{off}} \le u_{\text{off}_{\max}} \\ u_{\text{off}_{\min}} = \max(L_1, L_2, L_3, L_4) \\ u_{\text{off}_{\max}} = \min(U_1, U_2, U_3, U_4) \\ L_1 = -u_{pO}(u^{*}_{\max} - u^{*}_{\min})/u_{pn} \\ L_2 = -2u_{pO}(u^{*}_{\text{mid}} - u^{*}_{\min})/u_{pn} \\ L_3 = -2u_{\text{On}}(u_{pn} - u^{*}_{\max} + u^{*}_{\text{mid}})/u_{pn} \\ L_4 = -u_{\text{On}}(u_{pn} - u^{*}_{\max} + u^{*}_{\min})/u_{pn} \\ U_1 = u_{pO}(u_{pn} - u^{*}_{\max} + u^{*}_{\min})/u_{pn} \\ U_2 = 2u_{pO}(u_{pn} - u^{*}_{\text{mid}} + u^{*}_{\min})/u_{pn} \\ U_3 = 2u_{\text{On}}(u^{*}_{\max} - u^{*}_{\text{mid}})/u_{pn} \\ U_4 = u_{\text{On}}(u^{*}_{\max} - u^{*}_{\min})/u_{pn} \end{cases} \tag{19}$$

where $u_{\text{off}_{\min}}$ and $u_{\text{off}_{\max}}$ denote the lower and upper limits of the new zero-sequence voltage, respectively.

On the basis of (6)–(8), (17), and (18), the model of the neutral-point voltage is deduced as

$$\frac{d\bar{u}_{Og}}{dt} = \frac{u_{pn}(i_{\max} - i_{\min})u_{\text{off}}}{3C_F u_{pO} u_{\text{On}}} \approx \frac{0.84(i_{\max} - i_{\min})u_{\text{off}}}{C_F U_{\text{im}}}. \tag{20}$$

Obviously, the model described by (20) is a nonlinear system since a time-varying variable ($i_{\max}$-$i_{\min}$) is included. Thus a linearized model should be derived before the linear control theory is applied for designing the controller to balance neutral-point voltage conveniently. Considering the term ($i_{\max}$-$i_{\min}$) can be obtained by measurement, a new linearized model is constructed as

$$\begin{cases} \frac{d\bar{u}_{Og}}{dt} = \frac{0.84}{C_F U_{\text{im}}} u'_{\text{off}} \\ u'_{\text{off}} = (i_{\max} - i_{\min})u_{\text{off}} \end{cases} \tag{21}$$

where u'_{off} is the modified zero-sequence voltage. Equation (21) is treated as the plant model of the neutral-point voltage with the transfer function of the plant given by

$$G_p(s) = \frac{\bar{u}_{Og}(s)}{u'_{\text{off}}(s)} = \left(\frac{0.84}{C_F U_{\text{im}}}\right)\frac{1}{s}. \tag{22}$$

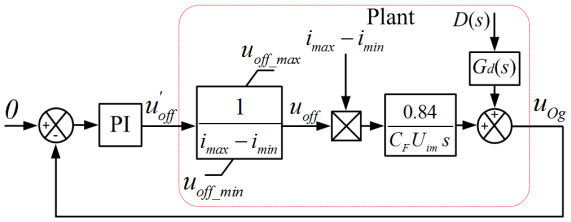

Fig. 5. Block diagram of the neutral-point voltage controller.

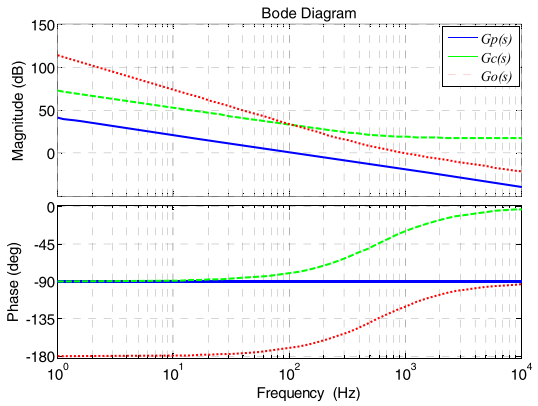

Fig. 6. Bode diagrams of the neutral-point voltage control loop.

B. Controller for Neutral-Point Voltage

It can be seen that a well-designed neutral-point voltage controller is essential for 3LT^{2}IMC since the capacitance of the filtering capacitor is small. Based on the plant model described in (22), a proportional-integral (PI) controller given by (23) is used in this paper

$$G_c(s) = K_p + \frac{K_i}{s} \tag{23}$$

where K_p is the proportional gain and K_i is the integration gain. And the open-loop transfer function of the control loop is derived as

$$G_o(s) = G_c(s)G_p(s) = \frac{0.84}{C_F U_{\text{im}}}\left(\frac{K_p s + K_i}{s^2}\right). \tag{24}$$

The block diagram of the controller is given in Fig. 5, where $D(s)$ is the disturbance in the control system and G_d (s) is the transfer function of the disturbance to the neutral-point voltage.

The selection of K_p and K_i is mainly based on the following considerations: 1) zero steady state error and 2) the gain crossover frequency f_c should be selected properly considering both the requirements of stability and dynamic response. Taking the factors such as the switching frequency into consideration, the crossover frequency of the control loop is selected as $f_c = f_s$ / 20 = 1 kHz and the phase margin is chosen as 60°. Therefore, the parameters of the PI controller are calculated as K_p = 7.68 and K_i = 27851. The bode diagrams of the control loop are shown in Fig. 6.

It is worth noting that the presented modulation strategy and neutral-point voltage control algorithm are generalized and can be extended to other three-level IMCs such

TABLE II
SYSTEM SPECIFICATIONS OF 3LT^{2}IMC

Parameters	Value
Power rating	1.5 *k*W
Input line-line voltage	220 Vrms
Input frequency f_n	50 Hz
Switching frequency f_s	20 *k*Hz
Inductor L_F	300 μH
Capacitor C_F	6.6 μF
Inductor L_v	1.2 *m*H
Inductor L_o	3 *m*H
Resistor R_L	25 ohm

as 3MC and three-level diode-clamped MC, since the methods are independent of specific dc source voltages. This can be performed according to their respective dc source voltages and therefore are not elaborated here, which are beyond the scope covered by this paper.

V. SIMULATION AND EXPERIMENTAL RESULTS

In this section, the system design of the 3LT^{2}IMC was presented first. Then to verify the correctness and feasibility of the proposed methods, the functionality and performance of 3LT^{2}IMC were first evaluated by simulation using MATLAB/Simulink software and then were validated experimentally.

A. System Design

1) Passive Components: Similar to the 3TSMC, proper design of the third-harmonic injection inductor is the key challenges to implement the converter [25]. The selection of the third-harmonic injection inductor should consider both the ripple current and current tracking performance. An inductor of large inductance is helpful to reduce the ripple current, but it makes the current response slow, and vice-versa. So a tradeoff should be made between these two aspects. According to the design criteria in [25], the range of the inductance of the third-harmonic injection inductor is determined by many system parameters, such as the amplitude of the input voltage, the switching frequency, the current ripple index, the power rating of the converter, and so on. By considering the system parameters listed in Table II, a 1.2 *m*H third-harmonic injection inductor is chosen, and the detailed design procedure is not elaborate here.

The input *LC* filter is mainly used for filtering the pulse currents generated by the converter and providing the instantaneous energy storage for the rear-end inverter such that three-phase sinusoidal input currents and proper operation of the converter can be achieved. The lower limit of the capacitance of the capacitor C_F is designed such that the voltage ripple of the capacitor can be limited to a certain level in order to prevent a distortion of the output voltage and enable safe operation of the converter. Besides, the upper limit of the capacitance of the capacitor should be selected based on the required input power factor at rated power. By considering the system parameters such as the power rating, the input voltage, the switching frequency and the desired input power factor, a 6.6 μF capacitor (2 parallel EPCOS MKP B32924 3.3 μF, 305 V film capacitors) is chosen. After selecting the capacitor, the input filtering inductor L_F is normally determined by the cutoff frequency of the input filter

$$L_F = \frac{1}{4\pi^2 f_{\text{cutoff}}^2 C_F}. \tag{25}$$

Generally, the cutoff frequency f_{cutoff} is designed as $f_{\text{cutoff}} = (0.1\text{–}0.2)\ f_s$. In this paper, a 300 μH inductor is selected.

2) Semiconductor Selection: The semiconductor switches are selected based on the voltage and current stresses. Considering a 220 Vrms input voltage, the 650 V insulated gate bipolar transistor (IGBT) devices are chosen here. The detailed analysis of the voltage and current stresses of the two-level 3TSMC has been presented in [25]. Thus this section mainly focuses on the selection of the bidirectional switches.

As the same as in conventional T-type three-level converters, the bidirectional switches S_{ay}, S_{by}, S_{cy}, S_{ro}, S_{so}, and S_{to} in the 3LT^{2}IMC topology need to conduct current in each direction and block voltage in both directions. In this paper, the bidirectional switches were implemented by an anti-series connection of two reverse-conducting IGBTs with common emitter configuration. On the other hand, the switching behavior and current stress of the switches S_{ay}, S_{by}, S_{cy} and the switches S_{ro}, S_{so}, S_{to} are quite different. Thus these two kinds of bidirectional switches should be selected based on their own features and requirements. As can be known from the operating principles of the 3LT^{2}IMC topology, the switches S_{ay}, S_{by}, S_{cy} of the third-harmonic injection circuit commutate at line-frequency and their current stresses are only half of the amplitude of the input current, thus the IGBT IKW30N65EL5 (650 V/30 A, Infineon) with low saturation voltage is chosen for the switches S_{ay}, S_{by}, S_{cy}. While for the switches S_{ro}, S_{so}, S_{to} of the three-level inverter, they commutate at high frequency and high current stress, thus high speed IGBT IKW40N65ES5 (650 V/40 A, Infineon) with both low switching losses and low saturation voltage is selected.

B. Simulation

Fig. 7 illustrates the capability of 3LT^{2}IMC producing three-phase multilevel outputs with controllable amplitude and frequency. The output parameters were set as $m_i = 0.5$, $f_o = 50$ Hz in Fig. 7(a), and $m_i = 0.9$, $f_o = 30$ Hz in Fig. 7(b), respectively, where f_o is the output frequency. The waveforms shown in Fig. 7 consist of the input phase voltage u_{sa}, the input current i_a, the output line-line voltage u_{rs} and the output current i_r. As can be seen from Fig. 7(a), the input current is nearly sinusoidal and in phase with the input phase voltage, except for a slight phase advance caused by the capacitive current drawn by the filtering capacitor. Thus, it is clear that 3LT^{2}IMC is able to generate sinusoidal input current and unity power factor at the input side. Of equal interest are the output waveforms, where a three-level output line-line voltage and a sinusoidal output current are observed. It can be seen from the envelope of the output line-line voltage

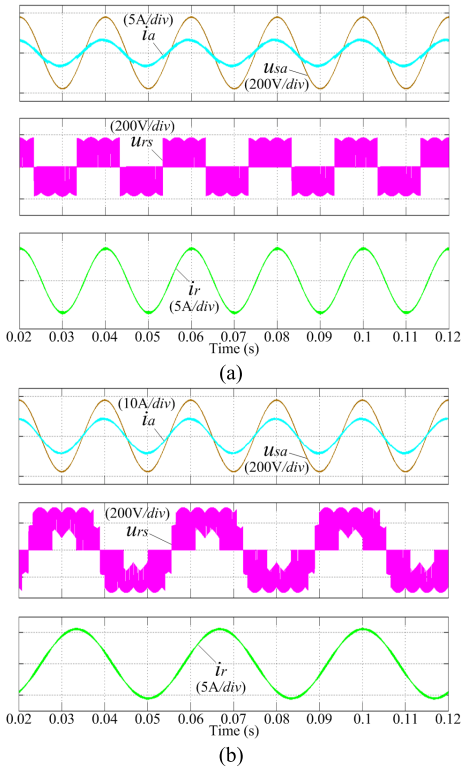

Fig. 7. Simulated waveforms of 3LT^{2}IMC with different m_i and f_o. (a) $m_i = 0.5$ and $f_o = 50$ Hz. (b) $m_i = 0.9$ and $f_o = 30$ Hz.

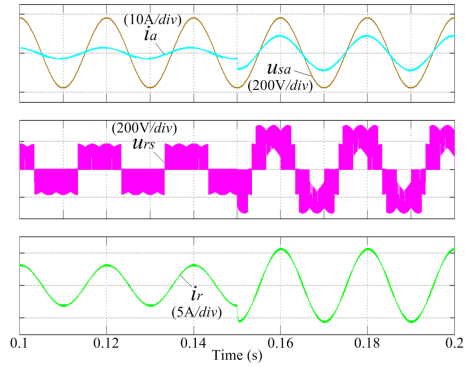

Fig. 8. Simulated waveforms of 3LT^{2}IMC in dynamic condition.

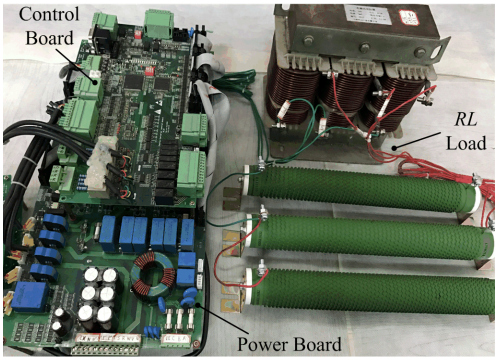

Fig. 9. Experimental setup of the 3LT^{2}IMC system.

that three distinctive levels including the upper dc voltage u_{pO}, the lower dc voltage u_{On} and the zero voltage, are used for synthesizing the output line-line voltage. This can be explained by the fact that, from the SVM perspective, only small vectors, medium vectors and zero vectors are used for producing the expected voltage vector at low modulation index.

As shown in Fig. 7(b), different from the three-level output line-line voltage in Fig. 7(a), a noticeable five-level output line-line voltage is generated in 3LT^{2}IMC. This is reasonable since five distinctive levels including the dc link voltage u_{pn}, the upper dc voltage u_{pO}, the lower dc voltage u_{On} and the zero voltage, are utilized for synthesizing the output voltages at high modulation index. Again, the desired features of sinusoidal input and output currents and unity power factor at the input side are achieved. Thus the results shown in Fig. 7 verified the correctness of the 3LT^{2}IMC topology and modulation strategies.

Fig. 8 shows the dynamic test of the system. In Fig. 8, the output frequency f_o is set as 50Hz, and the modulation index m_i is 0.5 at first. At 0.15s, m_i is step from 0.5 to 0.9. As can be seen from Fig. 8, the input and output currents are still sinusoidal, and the dynamic performance is good in the presented 3LT^{2}IMC system.

C. Experiments

To validate the theoretical analysis and simulation results, a laboratory prototype of 3LT^{2}IMC with the specifications given in Table II is built based on a configurable main circuit, as shown in Fig. 9. The control platform of 3LT^{2}IMC is implemented by a combination of floating-point digital signal processor TMS320F28335 and field-programmable gate array EP2C8T144C8N.

Fig. 10 demonstrates the experimental results of 3LT^{2}IMC generating three-phase multilevel outputs with different amplitudes and frequencies, and Fig. 11 shows the experimental results of 3LT^{2}IMC in dynamic condition. It is worth noting that the experimental results shown in Figs. 10 and 11 correspond to the simulated results shown in Figs. 7 and 8, and the experimental conditions and commands are exactly the same as those in the simulation. As can be seen from Figs. 10 and 11, the experimental results match the simulated results very well, except for a slight reduction in the amplitudes and higher distortions of the input and output currents. The higher distortions of the input and output currents in the experiments are attributed to the nonidealities of the power source (distortions and unbalance), the nonidealities of the power devices, the dead time effects, the narrow switching pulses, the measurement error of the transducers and the quantization error of the digital control system, etc. The input and output waveforms quality could be improved by optimizing the design of the prototype and the experimental conditions. Besides, it can be seen from Figs. 10 and 11 that the output voltage in the experiments contains some spikes. The spikes are mainly caused by the electro-magnetic interference noise picked up by the voltage probe and the screen persistence effect of the digital storage oscilloscope. Referring to Figs. 10 and 11, multilevel output line-line voltage and sinusoidal input and

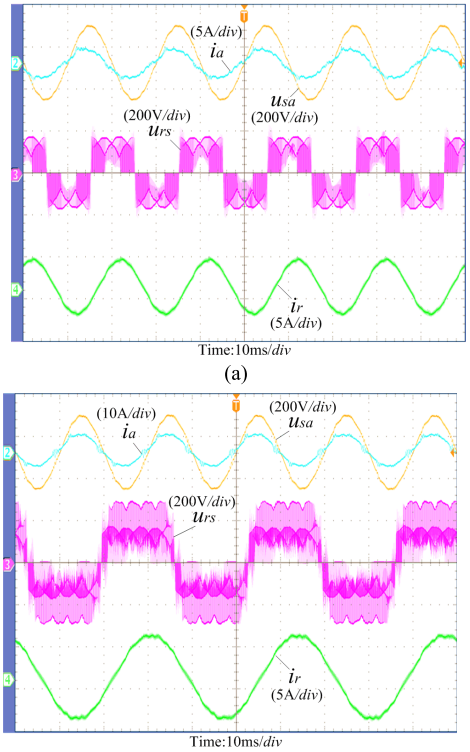

Fig. 10. Experimental waveforms of 3LT^{2}IMC with different m_i and f_o. (a) $m_i = 0.5$ and $f_o = 50$ Hz. (b) m_i =0.9 and $f_o = 30$ Hz. CH1 is the input phase voltage u_{sa}, CH2 is the input current i_a, CH3 is the output line-line voltage u_{rs}, CH4 is the output current i_r.

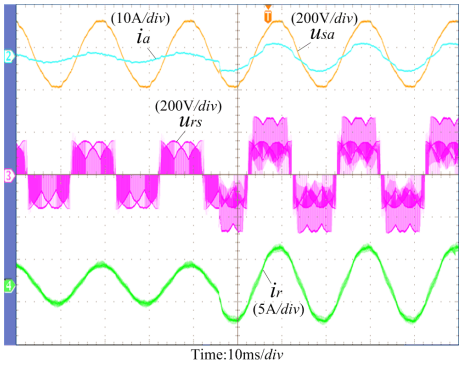

Fig. 11. Experimental waveforms of 3LT^{2}IMC in dynamic condition. CH1 is the input phase voltage u_{sa}, CH2 is the input current i_a, CH3 is the output line-line voltage u_{rs}, CH4 is the output current i_r.

output currents are achieved in the prototype, thus the validity of 3LT^{2}IMC is verified experimentally.

To verify the feasibility of the control algorithm for balancing the neutral-point voltage in the practical converter, the balancing capability under various operation conditions such as different modulation indices, different output frequencies and different loads, has been tested, and the results are shown in Fig. 12. The output parameters were set as follows: the modulation index m_i is set as 0.45 in Fig. 12(a) and 0.9 in Fig. 12(b) and (d); the output frequency f_o is set as 40 Hz in Fig. 12(a) and (b) and 60Hz in Fig. 12(c) and (d); the load is a series-connected *RL* branch ($R = 25$ ohm, $L = 3$ mH)

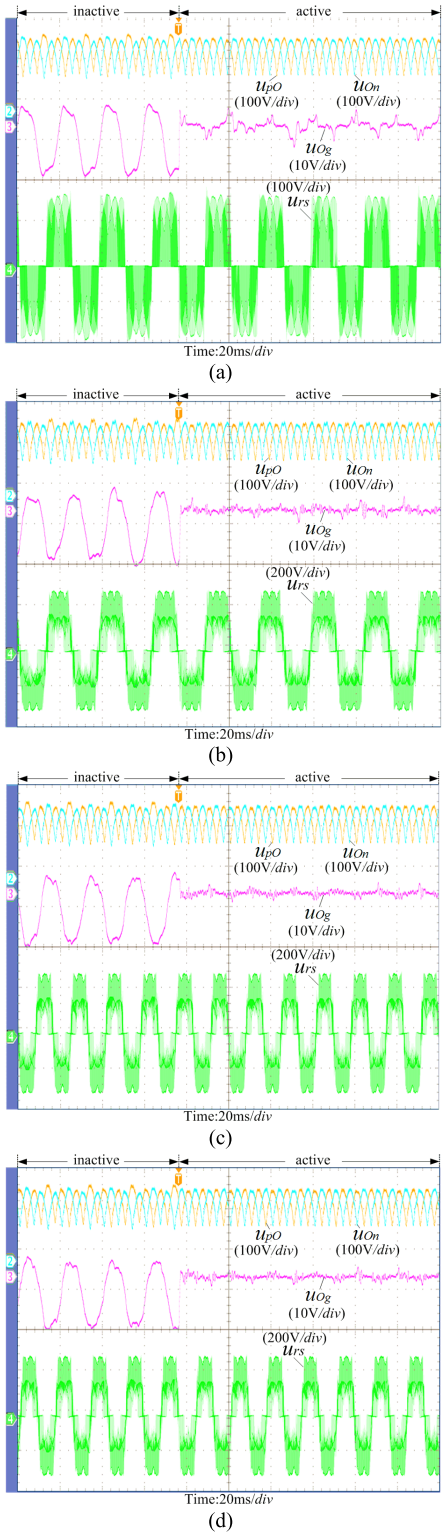

Fig. 12. Experimental results of neutral-point voltage balancing control under various operation conditions. (a) $m_i = 0.45$ and $f_o = 40$ Hz with *RL* load. (b) $m_i = 0.9$ and $f_o = 40$ Hz with *RL* load. (c) $m_i = 0.9$ and $f_o = 60$ Hz with *RL* load. (d) $m_i = 0.9$ and $f_o = 60$ Hz with *RLC* load. CH1 is the upper dcdc voltage u_{pO}, CH2 is the lower dc-dc voltage u_{On}, CH3 is the neutral-point voltage u_{Og}, and CH4 is the output line-line voltage u_{rs}.

in Fig. 12(a)–(c) and a *RLC* branch composed of a inductor in series with parallel-connected capacitor and resistor ($R = 25$ ohm, $L = 3$ mH, $C = 10\mu$F) in Fig. 12(d).

From the top to the bottom, the upper dc voltage u_{pO}, the lower dc voltage u_{On}, the neutral-point voltage u_{Og} and the output line-line voltage u_{rs} are shown sequentially in Fig. 12. In Fig. 12, the control algorithm was inactive at first and then was activated by an activation command. As can be seen from Fig. 12, before the control algorithm is activated, the neutral-point voltage of the practical converter is not zero. Instead, it exhibits low frequency oscillation, although zero averaged neutral-point current under ideal conditions is guaranteed by the developed modulation scheme. As a result, the upper and lower dc voltages are unbalanced, and the output line-line voltage is distorted. This can be seen from the uneven envelope of the output voltage. After activating the control algorithm, the neutral-point voltage is controlled to be almost zero and the upper and lower dc voltages become balanced. Thus the effectiveness of the balancing control algorithm under various operation conditions is verified experimentally.

D. Comparisons Between 3LT^{2}IMC and 3TSMC

Although it is difficult to make a very fair comparison between two different converter topologies, it is still worth giving a short qualitative assessment considering the basic performance of a converter in order to provide a general guideline for preselecting a suitable topology for dedicated application. In this paper, the performances of 3LT^{2}IMC and 3TSMC including the waveforms quality and converter efficiency, are evaluated and compared.

The input and output waveforms quality of 3LT^{2}IMC and 3TSMC at different modulation indices are evaluated, and the results are presented in Fig. 13. Fig. 13(a) and (c) show the input and output waveforms of 3LT^{2}IMC with the modulation indices being 0.45 and 0.9, respectively. As a comparison, the results of 3TSMC with the modulation indices being 0.45 and 0.9 are depicted in Fig. 13(b) and (d), respectively. The output frequency is set as 40 Hz and an *RL* load specified in Table II is used in Fig. 13. At a low-modulation index, shown in Fig. 13(a) and (b), 3LT^{2}IMC is able to synthesize the output line-line voltage with lower voltage levels. As shown in Fig. 13(a), the output line-line voltage of 3LT^{2}IMC is constructed by the input phase-to-neutral voltages instead of the input line-line voltages for 3TSMC, shown in Fig. 13(b). Consequently, the harmonic components in the output line-line voltage are reduced and a lower total harmonic distortion (THD) is achieved. By comparing Fig. 13(a) with 13(b), the dominant switching frequency related harmonics of the output line-line voltage of 3LT^{2}IMC are reduced from 11.2 to 10.7 V (f_s) and from 94.2 to 32.3 V ($2f_s$), and the THD of the output line-line voltage (THDu) is reduced significantly from 142.84% to 71.81%. While for the comparison of the input performance, the THD of the input current (THDi) of 3LT^{2}IMC is increased slightly from 8.87% to 11.61%. For the case of high modulation index, shown in Fig. 13(c) and (d), the output line-line voltage of 3LT^{2}IMC is clearly consist of five distinctive voltage levels instead of three voltage levels for 3TSMC. Compared with 3TSMC, the dominant switching frequency related harmonics of the output line-line voltage of 3LT^{2}IMC are reduced from 43.5 to 37.6 V (f_s) and from 67.7 to 53.6 V ($2f_s$), and the THDu and THDi are decreased from 72.36% to 49.32% and increased from 3.05% to 3.92%, respectively.

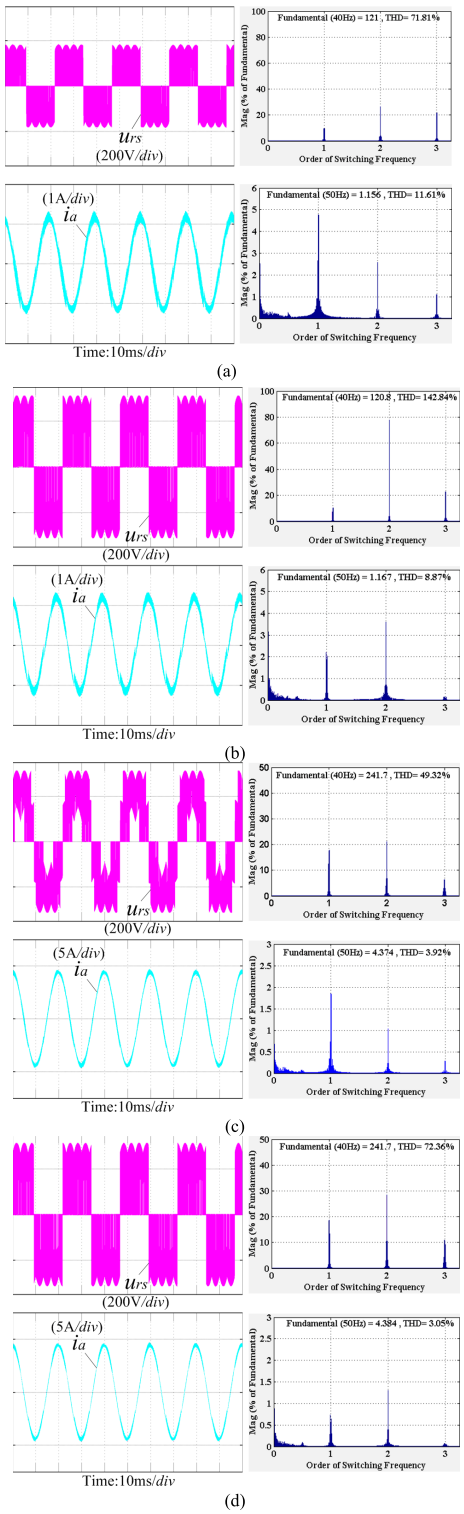

Fig. 13. Input and output performance comparisons between 3LT^{2}IMC and 3TSMC. (a) 3LT^{2}IMC with $m_i = 0.45$. (b) 3TSMC with $m_i = 0.45$. (c) 3LT^{2}IMC with $m_i = 0.9$. (d) 3TSMC with $m_i = 0.9$.

For both topologies, the THDu and THDi are measured and compared over the whole modulation indices range. The related results are shown in Fig. 14, where f_o is set as 40 Hz

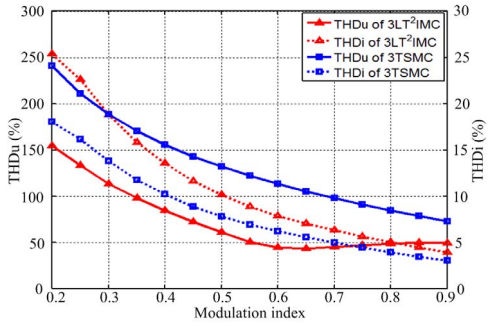

Fig. 14. THDs comparison between 3LT^{2}IMC and 3TSMC.

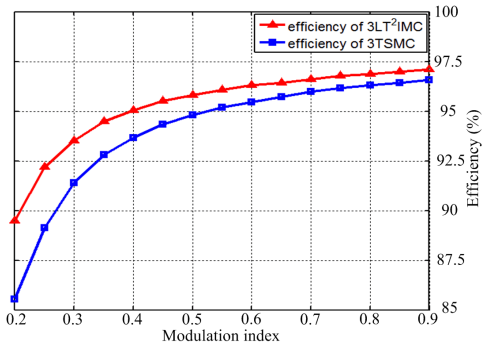

Fig. 15. Converter efficiency comparison between 3LT^{2}IMC and 3TSMC.

and the load specified in Table II is used. As can be seen from Fig. 14, 3LT^{2}IMC has a superior performance than 3TSMC in terms of THDu because of its multilevel output feature. However, in terms of the input current quality, 3TSMC is better than 3LT^{2}IMC, especially for lower modulation indices. This is mainly attributed to the presence of the neutral-point current in 3LT^{2}IMC. Based on the operating principles of 3LT^{2}IMC and 3TSMC, the input currents are synthesized by distributing the impressed dc link current accordingly to the input phases. From the SVM point of view, the use of small vectors in 3LT^{2}IMC disconnects the rectifier from one of the dc link and causes discontinuity in the dc link current. This increases the harmonic components of the input current and causes degradation of the input performance slightly.

In Fig. 15, the converter efficiency comparison between 3LT^{2}IMC and 3TSMC is carried out. Under the same operation conditions 3LT^{2}IMC shows higher converter efficiency when compared with 3TSMC. This can be explained by the fact that, although the conduct losses of the VSI of 3LT^{2}IMC are increased slightly, the switching losses of 3LT^{2}IMC are reduced significantly due to a lower commutation voltage, especially for high switching frequencies. In addition, due to the reduction of the harmonics at the outputs, losses in passive components such as the output inductors and the load machine can also be reduced, which leads to a further increase of the overall efficiency of 3LT^{2}IMC.

It can be found that, although the complexity in circuits and modulation strategies are increased slightly, 3LT^{2}IMC could provide an enhanced output power quality and higher efficiency when compared with 3TSMC, which makes 3LT^{2}IMC an attractive choice for the applications where high output power quality and excellent conversion efficiency are essential.

VI. Conclusion

In this paper, a three-level T-type indirect MC topology as well as a carrier-based modulation method is proposed. In addition to having the advantages such as extended input reactive power control range and no need for synchronization in modulation, 3LT^{2}IMC could provide an improved output power quality. To address the issue of neutral-point potential drift caused by the nonlinearities of the practical converter, a control algorithm for balancing the neutral-point voltage is presented. The developed modulation scheme and control algorithm are generalized and can be extended to other three-level IMCs. By applying the developed modulation scheme and control algorithm, 3LT^{2}IMC is able to synthesize multilevel output voltages and sinusoidal input currents simultaneously. Simulation and experimental results clearly show that 3LT^{2}IMC could achieve better output performance and higher converter efficiency than that of 3TSMC. By having sinusoidal input–output currents, improved output waveforms quality, high conversion efficiency and extended input reactive power control range, 3LT^{2}IMC is an attractive candidate for many applications such as WECS, FACTS and so on.

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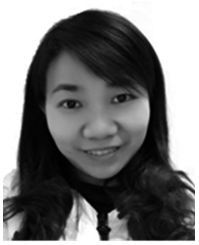

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